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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,130	11/14/2001	Ronald Hilton	AMDH-08152US0 DEL	4626

21603 7590 06/30/2005

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EXAMINER	
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ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,130	HILTON, RONALD	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 have been presented for examination based on the application filed on 14th November 2001.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

   The oath or declaration is defective because:
   a. It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.
   b. The clause regarding "willful false statements ..." required by 37 CFR 1.68 has been omitted.
   c. It does not identify the citizenship of each inventor.
   d. It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either on an application data sheet or supplemental oath or declaration.
   e. It was not executed in accordance with either 37 CFR 1.66 or 1.68.
   f. The full name of each inventor (family name and at least one given name together with any initial) has not been set forth.

3. Applicant is now required to submit a substitute declaration or oath to correct the deficiencies set forth above. The substitute oath or declaration must be filed within the THREE MONTH shortened statutory period set for reply in the "Notice of Allowability" (PTO-37). Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136. Failure to timely file the substitute declaration (or oath) will result in **ABANDONMENT** of the application. The transmittal letter

accompanying the declaration (or oath) should indicate the date of the "Notice of Allowance" (PTOL-85) and the application number in the upper right hand corner.

Drawings

4. The drawings are objected to because of the following:

   a. Fig.1: "Executable code 11" in the specification [0022] is not present in the drawing Fig.1. The executable code 10 is present in the drawing Fig.1 seems to be misnumbered.

   b. Fig.2: "Table 23" and "Translated Code Cache 22" in the figure are miss numbered according to the specification [0024].

   Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112, 2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims1,11,15 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.**

   Regarding Claim 1

   The omitted steps are: step of emulating execution of the legacy instruction and steps relating to the use of modified "store instruction" upon identification. As stated in the preamble the method steps should lead to the conclusion, as disclosed in the preamble. Method steps disclosed are merely translating and identifying legacy instruction as modified store instruction. Further, relationship between the step of translating and identifying the store instruction does not clearly satisfying the preamble.

   Claims 11, 15 and 25 are rejected for the same reasons as claim 1 rejection above.

6. **Claims1,11,15 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

   Regarding Claim 1

   The preamble in claim 1 and the subject matter that applicant claims to be his invention are not clearly tied together. Applicant discloses emulating execution of the legacy instruction in the preamble. As best understood by examiner, this merely

identifies the modified store instruction, but provides no further explanation as to how emulating the execution of this modified store instruction is any different than emulating the execution of any other legacy instruction.

Further, claim 1 has an incomplete decision tree. The claims discloses 3 level decision tree:

if the instruction is store instruction [Else omitted]

- if the afore mentioned instruction has instruction data [Else by pass check]

-- if the afore mentioned instruction data is modified [Else omitted]

Hence it is unclear what method steps are need in case "else" conditions are encountered. Further, it is unclear what happens when afore mentioned modified instruction data is identified (last if scenario).

Further, claim 1 is rejected, as examiner is not clear what exactly the phrase "translation information" encompasses. The specification discloses translation information only in the abstract and the claims, defining it with only providing "translation details". No further explanation on the translation information is provided. i.e. structure of the translation store (which is relied upon to determine if the instruction was translated), flags etc.

Further, claim 1 is rejected, as examiner is not clear what exactly the phrase "instruction data" encompasses. Does instruction data mean the operands of the store instruction or the complete instruction itself. The specification discloses instruction data in abstract, specification paragraphs [0010] [0031] & claims, but does not define it at any other place.

All of these structural inconstancies make the claim language vague and indefinite. Claims 11, 15 and 25 are rejected for the same reasons as claim 1 rejection above.

Claim Interpretation

7. Claim 1: "Indexing table", as best understood by examiner, is similar to the cache translation look-aside buffer (TLB), that indicates if the translation is present in the host code block (cache equivalent) on the cache.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-2, 4-10, 11-12, 15-16, 18-24 & 25-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding Claim 1

Claim 1 is non-statutory, as a human being could manually perform the steps defined in the method above. MPEP 2111 states:

> In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under 35 U.S.C. 101 and 102. In the 35 U.S.C. 102 rejection, the examiner explained that the claim was anticipated by a mental process augmented by pencil and paper markings. The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine. The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim,' to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.)

The method steps disclosed are further not tangibly embodied and do not produce a concrete (e.g. End-step of emulation execution and some result from execution) and tangible result (e.g. Computer display of the end of emulation execution on a non-native computer architecture) MPEP 2106 §II states:

> The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain

> some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.

Further, steps used in identifying the modification of instruction data in a store instructions, dictate the use of an algorithm. This algorithm does not seem to produce a concrete and tangible and merely identifies aforementioned modification. Further, these method steps can be performed on paper, as the disclosed algorithm is not associated directly the computer arts. Hence the claim is deemed non-statutory by the examiner. See MPEP 2106: Computer Related Inventions

> A process that merely manipulates an abstract idea or performs a purely mathematical algorithm is nonstatutory despite the fact that it might inherently have some usefulness. In Sarkar, 588 F.2d at 1335, 200 USPQ at 139, the court explained why this approach must be followed:
> No mathematical equation can be used, as a practical matter, without establishing and substituting values for the variables expressed therein. Substitution of values dictated by the formula has thus been viewed as a form of mathematical step. If the steps of gathering and substituting values were alone sufficient, every mathematical equation, formula, or algorithm having any practical use would be per se subject to patenting as a "process" under 101.
> Consideration of whether the substitution of specific values is enough to convert the disembodied ideas present in the formula into an embodiment of those ideas, or into an application of the formula, is foreclosed by the current state of the law.

The first & third rejection can be remedied by bringing the algorithm into the technological arts. Examiner respectfully suggest including the phrase like "Computer implemented method for emulation execution of legacy instructions..." in preamble. For the second rejection examiner respectfully suggests providing a concluding step that completes the emulation execution process. Further, providing the steps that connect the step of identifying the modified instruction data with the emulation execution process.

Claims 2 & 4-10 are rejected on the basis of their dependency on claim 1.

Claim 11 suffers from the same deficiencies as claim 1 and appropriate corrections are required. Claim 12 is rejected on the basis of their dependency on claim 11.

Claim 15 suffers from the same deficiencies as claim 1 and appropriate corrections are required.

Claims 16 & 18-24 are rejected on the basis of their dependency on claim 15.

Claim 25 suffers from the same deficiencies as claim 1 and appropriate corrections are required.

Claim 26 is rejected on the basis of their dependency on claim 25.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3, 7-9, 15-17 & 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6516295 issued to George A. Mann et al (Mann '295 hereafter).

Regarding Claim 1

Mann '295 teaches a method of emulating execution of a legacy instruction (Mann '295: Col.2 Lines 44-51). Mann '295 teaches instructions having instruction address (Mann '295: Col.5 Lines 28-29).

Further, **Mann '295** teaches accessing blocks of legacy instruction (Mann '295: Col.6 Lines 11-12). **Mann '295** teaches blocks having block addresses (Mann '295: Col.6 Lines 17-19).

Further, **Mann '295** teaches storing into translation store as the host code block (Mann '295: Fig. 3 Element 88; Col.5 Lines 58-63; Col.6 Lines 11-28) for each legacy instruction.

Further, **Mann '295** teaches storing translation indication at block numbers determined by block addresses (Mann '295: Fig. 3 Element 81). Mann '295 teaches

indexing table as block entry table for indicating that the block has been translated (Mann '295: Col.6 Lines 62-66).

Further, **Mann '295** teaches each particular legacy instruction of the translated block having a particular block number (Mann '295: Fig. 3 Element 72F-L, 80-81).

Further, **Mann '295'** teaches translating a particular legacy instruction into one or more translated instructions for emulating the particular legacy instruction (Mann '295: Col.6 Lines 53-55).

Further, Mann '295 teaches checking store instruction associated to the block entry table, if instruction data is stored for a particular block (Mann '295: Col.9 Lines 5-10). Mann '295 also teaches checking if the instruction data has been modified (Mann '295: Col.9 Lines 9 –20). Mann '295 teaches bypassing the checking if there is no store instruction data (Mann '295: Fig. 5 Element 134/136 & 148).

Regarding Claim 2

Mann '295 teaches the step of storing translation indications for only a subset of all translated blocks (Mann '295: Col.5 Lines 54-63).

Regarding Claim 3

Mann '295 storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Regarding Claim 7

Mann '295 teaches that legacy instructions are object code instructions compiled/assembled for the legacy architecture (Mann '295: Col.2 Lines 44-51).

Regarding Claim 8

Mann '295 teaches legacy instruction includes store instructions for modifying instruction code (Mann '295: Col.9 Lines 5-20, 38-47; Col.7 Lines 14-37).

Regarding Claim 9

Mann '295 teaches translation indication includes a state field as tag field, for each block number, indicating the block has been modified (Mann '295: Col.5 Table 1; Col.6 Lines 62-67).

Regarding Claim 15

Mann '295 teaches an apparatus and a method for emulating self-modifying code. The system claim 15 is directed towards the same limitations as the method claim 1 and is rejected for the same reason as claim 1.

Regarding Claim 16

The system claim 16 is directed towards the same limitations as the method claim 2 and is rejected for the same reason as claim 2.

Regarding Claim 17

The system claim 17 is directed towards the same limitations as the method claim 3 and is rejected for the same reason as claim 3.

Regarding Claim 21

The system claim 21 is directed towards the same limitations as the method claim 7 and is rejected for the same reason as claim 7.

Regarding Claim 22

The system claim 22 is directed towards the same limitations as the method claim 8 and is rejected for the same reason as claim 8.

Regarding Claim 23

The system claim 23 is directed towards the same limitations as the method claim 9 and is rejected for the same reason as claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 4-5, 10-13, 18-19 & 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6516295 issued to George A. Mann et al (Mann '295 hereafter) in view of ACM Article "Cache Memories" by Alan Jay Smith (Smith '1982 hereafter).

Regarding Claims 4 & 5

Teachings of Mann '295 are disclosed in the claim 1 rejection above. Indexing table as interpreted above is a TLB for a cache memory.

Mann '295 does not teach that the block numbers in the indexing table are the same for the multiple different subsets of blocks.

Smith '1982 teaches that TLB having a hashing mechanism to map the virtual addresses (block numbers) to the real address (translated host code block) (Smith '1982: Pg.475 Col.2 Paragraphs 3-4). Hashing (done by taking an XOR or through randomized algorithm) depends on the number of bits selected, resulting in folding or overlapping (Smith '1982: Pg.488, Col.1 Paragraph 1; Pg.489, Col.1). The hashing scheme selected by the applicant is extremely simplified version, as only one middle bit is selected to index the translation indication index table.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Smith '1982 and apply them to Mann '295 to implement the indexing table as disclosed. The motivation would have been that Smith '1982 discloses the necessity for TLB like lookup when dealing with translated information when address space doesn't map directly (Smith '1982: Pg.510, Section 2.9, 2.17). Mann '295's design requires translation as one target code block may have one or more translated host code instructions. Hence Smith '1982 solves Mann '295's problem of mapping the target legacy instruction object to translated host object code block (Mann '295: Col.6 Lines 47-55).

Regarding Claim 10

Mann '295 teaches the limitation "step of storing translation ... for multiple different blocks" as shown in the claim 4 rejection above.

Further, Mann '295 teaches storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Further, Mann '295 teaches that the translation indication includes a state field (tag field), for each block number, indicating the block has been modified (Mann '295: Col.5 Table 1; Col.6 Lines 62-67). Further, Mann '295 teaches incrementing the state field each time block is executed on the cache (Mann '295: Col.6 Lines 64-65).

It would have been obvious to keep track of modification to the block as modifications are already kept track at each legacy instruction level (Mann '295: Col.7 Lines 13-38).

Mann '295 does not teaches decrementing the count, but teaches equivalent functionality of removing and de-allocating the block entry table (indexing table entry) when the translated host block is no longer needed/garbage collected (Mann '295: Col.7 Lines 62-67, Col.8 Lines 1-3). Further, Mann '295 teaches bypassing the checking if there is no store instruction data (Mann '295: Fig. 5 Element 134/136 & 148).

Hence all limitation disclosed are either directly taught or obvious from Mann '295's disclosure in view of Smith '1982. The motivation to combine is the same as state in claims 4-5 rejection above.

Regarding Claim 11

Teachings of **Mann '295** are shown in claim rejection for claims 1-3,4 & 9 above. They are repeated here for clarity of prosecution.

Mann '295 teaches a method of dynamic emulating execution of a legacy instruction (Mann '295: Col.2 Lines 44-51). Mann '295 teaches instructions having instruction address (Mann '295: Col.5 Lines 28-29). Further, **Mann '295** teaches accessing

blocks of legacy instruction (Mann '295: Col.6 Lines 11-12). **Mann '295** teaches blocks having block addresses (Mann '295: Col.6 Lines 17-19). Further, **Mann '295** teaches storing translated code into host code block (translation store) for each legacy instruction (Mann '295: Fig. 3 Element 88; Col.5 Lines 58-63; Col.6 Lines 11-28).

Further, **Mann '295** teaches storing translation indication at block numbers determined by block addresses (Mann '295: Fig. 3 Element 81). Mann '295 teaches indexing table as block entry table for indicating that the block has been translated (Mann '295: Col.6 Lines 62-66). Further, **Mann '295** teaches each particular legacy instruction of the translated block having a particular block number (Mann '295: Fig. 3 Element 72F-L, 80-81).

Further, **Mann '295** teaches translating a particular legacy instruction into one or more translated instructions for emulating the particular legacy instruction (Mann '295: Col.6 Lines 53-55). Further, Mann '295 teaches checking store instruction associated to the block entry table, if instruction data is stored (Mann '295: Col.9 Lines 5-10) for a particular block. Mann '295 also teaches checking if the instruction data has been modified (Mann '295: Col.9 Lines 9 –20). Further, Mann '295 teaches bypassing the checking if there is no store instruction data (Mann '295: Fig. 5 Element 134/136 & 148). Further, **Mann '295** teaches the step of storing translation indications for only a subset of all translated blocks (Mann '295: Col.5 Lines 54-63). **Mann '295** teaches storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Teachings pertaining to claim 4 limitations are disclosed above.

Mann '295 teaches translation indication includes a state field as tag field for each block number indicating the block has been modified (Mann '295: Col.5 Table 1; Col.6 Lines 62-67).

Motivation to combine the teachings of Mann '295 with Smith '1982 is the same as claim 4-5 motivations disclosed above.

Regarding Claim 12

Method claim 12 is directed towards the same limitations as the method claim 10 and is rejected for the same reason as claim 10.

Regarding Claim 13

Mann '295 teaches that legacy instructions are object code instructions compiled/assembled for the native legacy architecture executed as guest on host architecture (Mann '295: Col.2 Lines 44-51, Fig.3).

Regarding Claim 18

The system claim 18 is directed towards the same limitations as the method claim 4 and is rejected for the same reason as claim 4.

Regarding Claim 19

The system claim 19 is directed towards the same limitations as the method claim 5 and is rejected for the same reason as claim 5.

Regarding Claim 24

The system claim 24 is directed towards the same limitations as the method claim 10 and is rejected for the same reason as claim 10.

Regarding Claim 25

The system claim 25 is directed towards the same limitations as the method claim 11 and is rejected for the same reason as claim 11.

Regarding Claim 26

The system claim 26 is directed towards the same limitations as the method claim 10 and is rejected for the same reason as claim 10.

Regarding Claim 27

The system claim 27 is directed towards the same limitations as the method claim 13 and is rejected for the same reason as claim 13.

11. Claims 6 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,516,295 issued to George A. Mann et al (Mann '295 hereafter) in view of U.S. Patent No. 5,560,013 issued to Casper A. Scalzi et al (Scalzi '013 hereafter).

Regarding Claim 6

Teachings of Mann '295 are disclosed in the claim 1 rejection above.

Mann '295 does not teach legacy instructions are for a legacy system having S/390 Architecture.

Scalzi '013 teaches that legacy instructions are for a legacy system having S/390 Architecture (Scalzi '013: Col.17 Lines 54-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Scalzi '013 and apply them to Mann '295 to emulate execution of legacy instruction for S/390 legacy architecture. The motivation would have been that Scalzi '013 and Mann '295 are analogous art and Scalzi '013 is performing the instruction set translation in a very similar fashion as Mann '295 through mapping/dynamic address translation (Scalzi '013: Col. 5 Lines 17-23) and instruction-self-modification (Scalzi '013: Col.12 Lines11-24; Col.14 Lines 16-24).

Regarding Claim 20

The system claim 20 is directed towards the same limitations as the method claim 6 and is rejected for the same reason as claim 6.

12. Claims 14 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,516,295 issued to George A. Mann et al (Mann '295 hereafter) in view of ACM Article "Cache Memories" by Alan Jay Smith (Smith '1982 hereafter), further in view of U.S. Patent No. 5,560,013 issued to Casper A. Scalzi et al (Scalzi '013 hereafter).

Regarding Claim 14

Teachings of Mann '295 & Smith '1982 are disclosed in the claim 11 rejection above.

Mann '295 & Smith '1982 do not teach emulated execution by translation from CISC based legacy instruction set to the RISC based target/host instruction set.

Scalzi '013 teaches that legacy instructions are for a legacy system having S/390 Architecture which is a CISC architecture and host architecture is power PC (RISC) based architecture (Scalzi '013: Col.17 Lines 54-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Scalzi '013 and apply them to Mann '295 to emulate execution of legacy instruction for S/390 legacy architecture. The motivation would have been that Scalzi '013 and Mann '295 are analogous art and Scalzi '013 is performing the instruction set translation in a very similar fashion as Mann '295 through mapping/dynamic address translation (Scalzi '013: Col. 5 Lines 17-23) and instruction-self-modification (Scalzi '013: Col.12 Lines11-24; Col.14 Lines 16-24).

Regarding Claim 28

Teachings of Mann '295 & Smith '1982 are disclosed in the claim 25 rejection above. The system claim 28 is directed towards the same limitations as the method claim 14 and is rejected for the same reason as claim 14. To facilitate prosecution rejection is repeated below.

Mann '295 & Smith '1982 do not teach emulated execution by translation from CISC based legacy instruction set to the RISC based target/host instruction set.

Scalzi '013 teaches that legacy instructions are for a legacy system having S/390 Architecture which is a CISC architecture and host architecture is power PC, RISC based architecture (Scalzi '013: Col.17 Lines 54-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Scalzi '013 and apply them to Mann '295 to emulate execution of legacy instruction for S/390 legacy architecture. The motivation would have been that Scalzi '013 and Mann '295 are analogous art and Scalzi '013 is performing the instruction set translation in a very similar fashion as Mann '295 through mapping/dynamic address translation (Scalzi '013: Col. 5 Lines 17-23) and instruction-self-modification (Scalzi '013: Col.12 Lines11-24; Col.14 Lines 16-24).

13. Claims 8 & 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,516,295 issued to George A. Mann et al (Mann '295 hereafter) in view of applicant's own admission in the specification.

Regarding Claim 8 & 22

Teachings of Mann '295 are disclosed in the claim 1 rejection above.

Mann '295 teaches legacy instruction includes store instructions for modifying instruction code.

Further, by applicant's own admission the processing of self-modifying instruction is well known in the art and handled inherently even by system which don't facilitate dynamic code self-modification (Specification: [0028]).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of applicant and Mann '295. The motivation to combine would be that applicant admits knowing out the store instruction to modify the instruction code and Mann '295 provides further proof of stated fact.

Remarks

14. All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 24, 2005

JEAN R. HOMERE
PRIMARY EXAMINER